CLAIMS

What is Claimed is:

1. A semiconductor device package (10) configured for electrical connection to an external circuit, the semiconductor device package (10) comprising:

a package body (30);

a semiconductor device (12) disposed within the package body (30);

at least one passive device (14) disposed within the package body (30); and

a lead frame (17) formed from electrically conductive material, the lead frame (17) including:

a plurality of leads (16) electrically connected to I/O pads (22) on the semiconductor device (12), each of the leads (16) including a first surface (38) exposed from the package body (30) for electrical connection to the external circuit, and

a plurality of first interposers (20) electrically connected to the at least one passive device (14), at least one interposer (20) in the plurality of interposers (20) being electrically connected to at least one lead (16) in the plurality of leads (16) for electrically connecting the at least one passive device (14) with the external circuit.

2. The semiconductor device package (10) of claim 1, wherein the package body (30) is formed by a molding compound (28) encapsulating at least a portion of the semiconductor die (12), at least a portion of the at least one passive component (14), and at least a portion of the lead frame (17).

3. The semiconductor device package (10) of claim 2, wherein the first surfaces (38) of the leads (16) are exposed substantially coplanar with a surface (34) of the package body (30).

4. The semiconductor device package (10) of claim 1, wherein the at least one passive device (14) is selected from the group consisting of capacitors, inductors, and resistors.

5. The semiconductor device package (10) of claim 1, wherein the lead frame (17) further includes a die pad (54), the semiconductor device (12) being secured to the die pad (54).

6. The semiconductor device package (10) of claim 1, wherein a portion of the semiconductor device (12) is exposed from the package body (30).

7. The semiconductor device package (10) of claim 1, wherein the I/O pads (22) on the semiconductor device (12) are soldered to bond sites (124) on the lead frame (17) for forming a flip-chip attachment.

8. The semiconductor device package (10) of claim 7, wherein the bond sites (124) are formed on second interposers (122) connected to the plurality of leads (16).

9. The semiconductor device package (10) of claim 8, wherein the second interposers (122) each include a support post (128) disposed beneath the bond sites (124), the support posts (128) being exposed at a surface (34) of the package body (10).

10. The semiconductor device package (10) of claim 8, wherein the at least one interposer (20) in the plurality of interposers (20) is electrically connected to at least one lead (16) in the plurality of leads (16) by at least one third interposer (126).

11. The semiconductor device package (10) of claim 1, wherein the I/O pads (22) on the semiconductor device (12) are wire bonded or tape bonded to the plurality of leads (16).

12. The semiconductor device package (10) of claim 1, wherein at least one of the first interposers (20) in the plurality of first interposers (20) includes a support post (58) extending therefrom, the support post (58) being exposed at a surface (34) of the package body (10).

13. A semiconductor device package (10) comprising:

a molding compound (28) forming at least a portion of a first package face (34);

at least one passive device (14) at least partially covered by the molding compound (28);

a semiconductor device (12) at least partially covered by the molding compound (28), the semiconductor device (12) including a plurality of I/O pads (22); and

a lead frame formed (17) from electrically conductive material and partially covered by the molding compound (28), the lead frame (17) including:

a plurality of leads (16), each having a first surface forming a bond site electrically connected to at least one I/O pad (22) in the plurality of I/O pads (22) and a second surface (38) exposed at the first package face (34), and

a plurality of first interposers (20) electrically connected to at least one passive device (14), the plurality of first interposers (20) each having a third surface coplanar with the first surfaces of the plurality of leads (16), at least a portion of each first interposer (20) in the plurality of first interposers (20) being spaced apart from the first package face (34).

14. The semiconductor device package (10) of claim 13, wherein the at least one passive device (14) is selected from the group consisting of capacitors, inductors, and resistors.

15. The semiconductor device package (10) of claim 13, wherein the lead frame (17) further includes a die pad (54), the semiconductor device (12) being secured to the die pad (54).

16. The semiconductor device package (10) of claim 13, wherein a portion of the semiconductor device (12) is exposed at the first package face (34).

17. The semiconductor device package (10) of claim 13, wherein the I/O pads (22) on the semiconductor device (12) are soldered to bond sites (124) on the lead frame (17) for forming a flip-chip attachment.

18. The semiconductor device package (10) of claim 17, wherein the bond sites (124) are formed on second interposers (122) connected to the plurality of leads (16).

19. The semiconductor device package (10) of claim 18, wherein the second interposers (122) each include a support post (128) disposed beneath the bond sites (124), the support posts (128) being exposed at the first package face (34).

20. The semiconductor device package (10) of claim 13, wherein at least one of the first interposers (20) in the plurality of first interposers (20) includes a support post (58) extending therefrom, the support post (58) being exposed at the first package face (34).

21. The semiconductor device package (10) of claim 13, wherein the I/O pads (22) on the semiconductor device (12) are wire bonded or tape bonded to the plurality of leads (16).

22. The semiconductor device package (10) of claim 13, wherein at least one lead (16) in the plurality of leads (16) is electrically connected to at least one first interposer (20) in the plurality of first interposers (20).

23. A method of forming a semiconductor device package (10), the method comprising:

forming a lead frame (17) from an electrically conductive material, including:

forming a plurality of leads (16) and a plurality of first interposers (20) in the conductive material, and

etching a bottom surface of the plurality of leads (16) and the plurality of interposers (16), the etching defining a plurality of first surfaces (38) on the contacts (16);

electrically connecting I/O pads (22) on a semiconductor device (12) to the plurality of leads (16);

electrically connecting at least one passive device (14) across pairs of first

interposers (20) in the plurality of first interposers (20); and

covering at least a portion of each of the lead frame (17), the semiconductor device (12), and the at least one passive device (14) with a molding compound (28), the molding compound (28) forming at least a portion of a first package face (34), wherein the first surface (38) of each lead (16) is exposed at the first package face (34) and at least a portion of each first interposer (20) is spaced apart from the first package face (34).

24. The method of claim 23, wherein the at least one passive device (14) is selected from the group consisting of capacitors, inductors, and resistors.

25. The method of claim 23, wherein forming the lead frame (17) further includes forming a die pad (54) from the electrically conductive material, and the method further comprises:

securing the semiconductor device (12) to the die pad (54).

26. The method of claim 23, wherein a portion of the semiconductor device (12) is exposed at the first package face (34).

27. The method of claim 23, wherein electrically connecting the I/O pads (22) on the semiconductor device (12) to the plurality of leads (16) includes:

soldering the I/O pads (22) to bond sites (124) on the lead frame (17) for forming a flip-chip attachment.

28. The method of claim 27, wherein forming the lead frame (17) further includes forming a plurality of second interposers (122) connected to the plurality of leads (16) , the bond sites (124) being formed on the second interposers (122).

29. The method of claim 28, wherein the etching further defines support posts (128) disposed beneath the bond sites (124) on the second interposers (122), the support posts (128) being exposed at the first package face (34) after the covering with the molding compound (28).

30. The method of claim 23, wherein the etching further defines a support post (58) extending from at least one of the first interposers (20) in the plurality of first interposers (20), the support post (58) being exposed at the first package face (34) after the covering with the molding compound (28).

31. The method of claim 30, further comprising:

adhering the support post (58) and the first surface (38) of each lead (16) to a surface (100) before covering with the molding compound (128).

32. The method of claim 23, wherein electrically connecting the I/O pads (22) on the semiconductor device (12) to the plurality of leads (16) includes:

wire bonding or tape bonding the I/O pads (22) to the plurality of leads (16).

33. The method of claim 23, further comprising:

electrically connecting at least one lead (16) in the plurality of leads (16) to at least one first interposer (20) in the plurality of first interposers (20).